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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,750	11/21/2003	Sailesh Kottapalli	42P17886	1829

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EXAMINER	
LAI, VINCENT	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,750	KOTTAPALLI, SAILESH	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EX...
TECHNOLOGY CENTER
9/18/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Acknowledgment is made of amendments to claims, title, drawings, and specification.

2. Objections to claims, drawings and title are withdrawn after considering amendments.

Response to Arguments

3. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Gschwind (U.S. Patent # 6,189,088 B1).

As per **claim 1**, Gschwind et al discloses a method, comprising:

issuing an advanced load instruction (See column 13, lines 18-20: Out-of-order loads included advanced loads) with a first instance of a first destination register (See column 9, lines 49-52: Disclosure of a destination register);

decoding (Instructions are inherently decoded) a test instruction (See column 15, lines 14-18: A 'check address interference and conditional load register' instruction is a test instruction) with a second instance of said first destination register where said second instance of said first destination register is decoded as a first source register (See column 15, lines 21-25: Such is the case when a register match occurs);

register renaming said first instance of said first destination register and said first source register to a first physical register (See column 20, lines 18-22: Register renaming is used); and

validating results of said advanced load instruction using said test instruction with said first physical register (See column 15, lines 14-52: The test instruction tries to validate the load).

As per **claim 2,** Gschwind et al discloses wherein said test instruction is a load conditional instruction with said second instance of said first destination register (See column 15, lines 14-52: The test instruction tries to validate the load with a load).

As per **claim 3**, Gschwind et al discloses further comprising register renaming said second instance of said first destination register to a second

physical register (See column 21, lines 3-7: Registers are renamed according to the register map table).

As per **claim 4**, Gschwind et al discloses wherein said test instruction operates to move contents of said first physical register to said second physical register when said validation indicates said results are valid (See column 21, lines 3-14: Registers are updated with assignment).

As per **claim 5**, Gschwind et al discloses wherein said test instruction is a speculation check instruction with said second instance of said first destination register (See column 16, lines 13-16: Indicative of handling cases when a speculation results in a conflict).

As per **claim 6**, Gschwind et al discloses wherein said validating includes searching a table for an entry with said first physical register (See column 16, lines 13-16: The register map table is used and referenced when making decisions for updating).

As per **claim 7**, Gschwind et al discloses a processor, comprising:

a decoder (Decoders are inherent in a processor) to decode a test instruction (See column 15, lines 14-18: A 'check address interference and conditional load register' instruction is a test instruction) with a first instance of a first destination register corresponding to an advanced load instruction with a

second instance of said first destination register wherein said first instance is decoded as a first source register (See column 15, lines 21-25: Such is the case when a register match occurs); and

a register renaming stage to rename said second instance of said first destination register and said first source register to a first physical register (See column 20, lines 18-22: Register renaming is used).

As per **claim 8**, Gschwind et al discloses wherein said test instruction is a load conditional instruction (See column 15, lines 14-52: The test instruction tries to validate the load with a load).

As per **claim 9**, Gschwind et al discloses wherein said register renaming stage to rename said first instance of said first destination register to a second physical register (See column 21, lines 3-7: Registers are renamed according to the register map table).

As per **claim 10**, Gschwind et al discloses wherein said load conditional instruction operates to move contents of said first physical register to said second physical register when a validation circuit indicates that results of said advanced load instruction are valid (See column 21, lines 3-14: Registers are updated with assignment).

As per **claim 11**, Gschwind et al discloses wherein said validation circuit includes an advanced load address table (See figure 4).

As per **claim 12**, Gschwind et al discloses wherein said test instruction is a speculation check instruction (See column 15, lines 14-18: A 'check address interference and conditional load register' instruction is a test instruction).

As per **claim 13**, Gschwind et al discloses wherein said speculation check instruction is a no-operation when a validation circuit indicates that results of said advanced load instruction are valid (See column 15, lines 14-52: Bypassing is done when valid).

As per **claim 14**, Gschwind et al discloses wherein said validation circuit is an advanced load address table (See figure 4).

As per **claims 15-20**, Gschwind discloses the limitations of the claims for similar reasoning found for claims 1-6.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

> said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gschwind (U.S. Patent # 5,625,837), in view of Witt et al (U.S. Patent # 6,189,068 B1), herein referred to as Witt.

As per **claim 21-28**, Gschwind teaches a system, comprising the processor of claims 7-14.

Gschwind does not teach an interface for input-output devices, specifically an audio input-output circuit.

Witt does teach an interface to couple said processor to input-output devices (See column 193, lines 15-17: An interface is described), and an audio input-output circuit coupled to said interface and to said processor (See claim 13, column 196, lines 21-22).

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Gschwind by the teachings of Witt et al to include an interface for input-output devices, specifically an audio input-output circuit, because such changes will allow the introduction of peripheral instructions and data to the processor through additions of ports and/or buses to the existing architecture; and having an interface for input-output devices can "enhance the performance of computer system" (See Witt on the inclusion of I/O devices, column 193, lines 19-21). Further, interfaces for input-output devices, including an interface for audio, is also recognized as common

practice for computer systems/processors at the time of the invention and is well known by people having ordinary skill in the art. Although a computer system/processor may be made to interact with itself only, one that includes the ability to communicate with peripheral devices is more commonplace and useful.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the art with respect to the method and apparatus for data speculation in an out-of-order processor utilizing test instructions and register renaming:

U.S. Patent # 5,625,837 to Popescu et al shows a processor architecture having out-of-order execution, speculative branching, and giving priority to instructions which affect a condition code.

U.S. Patent # 5,815,688 to Averill shows a verification of accesses in a functional model of a speculative out-of-order computer system.

U.S. Patent # 5,841,998 to Isaman shows a system and method of processing instructions for a processor.

U.S. Patent # 5,854,921 to Pickett shows a stride-based data address prediction structure with validation and correction circuitry.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

vl
September 14, 2006

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9/12/2006